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EXAMINER	
CHRISTENSEN, SCOTT B	
ART UNIT	**PAPER NUMBER**
2144	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,747	NARAD, CHARLES E.	
	Examiner	Art Unit	
	Scott Christensen	2144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/30/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in regards to the most recent papers filed on 1/10/2007.

Response to Arguments

2. Applicant's arguments with respect to claims 1-38 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in US Patent number 6,434,620 B1.

With regard to claim 1, Boucher discloses a network interface comprising: circuitry to receive and transmit network data (Boucher: Abstract. The INIC and CPD works with a host computer for data communication); a direct memory access unit (Boucher: Column 8, lines 32-38); circuitry to maintain at least one statistic metering operation of the network interface (Boucher: Column 44, lines 20-23. As the INIC has the exact values for certain statistics, circuitry must exist to maintain the statistic); circuitry, operationally coupled to the direct memory access unit, to initiate direct

memory access transfer of at least one of the at least one statistic metering operation of the network interface (Boucher: Column 63, lines 17-43. The Utility CPU utilizes DMA, and the Utility CPU is responsible for requests of statistics –Boucher: Column 56, lines 27-33). Boucher does not disclose expressly that the circuitry to initiate direct memory access transfer initiates direct memory transfer in response to at least one selected from the group of: (1) at least one configured time interval, and (2) when at least one of the at least one statistic reaches a configured threshold.

A person of ordinary skill in the art would have known how to have the circuitry to initiate direct memory access transfer initiates direct memory transfer in response to at least one selected from the group of: (1) at least one configured time interval, and (2) when at least one of the at least one statistic reaches a configured threshold in the network interface of Boucher.

Evidence of this can be found in Nichols et al. in US Patent 4,875,206, hereafter referred to as "Nochols." Nichols discloses a system with time slots, where every fifth time slot is used to send control messages. This means that a DMA transmissions can only be initiated after the fifth time slot, when the control messages are sent to set up the DMA session (Nichols: Column 3, lines 9-29).

It would have been obvious to have the circuitry to initiate direct memory access transfer initiates direct memory transfer in response to at least one configured time interval in the network interface of Boucher.

The suggestion/motivation for doing so would have been that allowing DMA transfers only at specific intervals prevents DMA transfers from conflicting with other

system functions. By delaying the transfer of the statistics, the transfer of the statistics is less likely to cause conflicts with other components, as time slots can be utilized to properly schedule each component.

With regard to claims 16, Boucher discloses a method comprising maintaining statistics at a network interface metering operation of the network interface (Boucher: Column 44, lines 20-23. As the INIC has the exact values for certain statistics, circuitry must exist to maintain the statistic), and transferring by direct memory access from the network interface to a memory accessed by at least one processor at least one of the statistics metering operation of the network interface (Boucher: Column 63, lines 17-43. The Utility CPU utilizes DMA, and the Utility CPU is responsible for requests of statistics –Boucher: Column 56, lines 27-33). Boucher does not disclose expressly that the transfer is in response to at least one statistic reaching a configured threshold.

A person of ordinary skill in the art would have known how to have the transfer being in response to at least one statistic reaching a configured threshold. It would have been obvious to have the transfer being in response to at least one statistic reaching a configured threshold.

The suggestion/motivation for doing so would have been that the statistics would most likely be represented by a limited number of bits. This causes the statistics to have a cap based on the number of bits that are used for representing the statistics (i.e. 8 bits would cause the statistic to be capped at 255 while 16 bits would limit the statistic at 65,535). No matter how much bits are used to represent the statistics, there is always an upper cap to the network interface's ability to represent the statistic in

memory. Once the cap is reached, there would be four feasible options. First, zero out the statistic (rollover the counter). Second, initiate an overflow type error and discontinue incrementing the statistic. Third, stop incrementing the statistic (so the statistic would stay at maximum). Fourth, transfer the statistic and zero out the memory locations that were storing the statistic, and process the statistic or store it in a memory location that is most likely far larger than that which is allocated on the network interface. As the fourth option is the only option that allows the counting to continue while preserving the old data, a person of ordinary skill in the art would be most motivated to choose this option.

With regard to claims 26, Boucher discloses a program comprising maintaining statistics at a network interface metering operation of the network interface (Boucher: Column 44, lines 20-23. As the INIC has the exact values for certain statistics, circuitry must exist to maintain the statistic), and transferring by direct memory access from the network interface to a memory accessed by at least one processor at least one of the statistics metering operation of the network interface (Boucher: Column 63, lines 17-43. The Utility CPU utilizes DMA, and the Utility CPU is responsible for requests of statistics –Boucher: Column 56, lines 27-33). Boucher does not disclose expressly that the transfer is in response to at least one configured time interval.

A person of ordinary skill in the art would have known how to have the transfer be in response to at least one configured time interval.

Evidence of this can be found in Nichols. Nichols discloses a system with time slots, where every fifth time slot is used to send control messages. This means that a

DMA transmissions can only be initiated after the fifth time slot, when the control messages are sent to set up the DMA session (Nichols: Column 3, lines 9-29).

It would have been obvious to have the transfer be in response to at least one configured time interval.

The suggestion/motivation for doing so would have been that allowing DMA transfers only at specific intervals prevents DMA transfers from conflicting with other system functions. By delaying the transfer of the statistics, the transfer of the statistics is less likely to cause conflicts with other components, as time slots can be utilized to properly schedule each component.

With regard to claim 34, Boucher discloses a system comprising:

(1) At least one processor (Boucher: Column 3, lines 28-43);

(2) Memory operationally coupled to the at least one processor (Boucher: Column 61, lines 14-30);

(3) A network interface comprising: circuitry to receive and transmit data over a network connection (Boucher: Column 6, line 60 to column 7, line 10); a direct memory access unit operationally coupled to the memory (Boucher: Column 8, lines 32-38); circuitry to maintain statistics metering operation of the network interface (Boucher: Column 44, lines 20-23. As the INIC has the exact values for certain statistics, circuitry must exist to maintain the statistic); circuitry operationally coupled to the direct memory access unit to initiate direct memory access transfer of multiple ones of the statistics metering operation of the network interface (Boucher:

Column 63, lines 17-43. The Utility CPU utilizes DMA, and the Utility CPU is responsible for requests of statistics –Boucher: Column 56, lines 27-33); the statistics comprising at least one of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface (Boucher: Column 56, lines 51-63).

Boucher does not disclose expressly that the circuitry to initiate direct memory access transfer initiates direct memory access transfer in response to a schedule of times to initiate the transfer.

A person of ordinary skill in the art would have known how to have the circuitry to initiate direct memory access transfer initiates direct memory access transfer in response to a schedule of times to initiate the transfer.

Evidence of this can be found in Nichols. Nichols discloses a system with time slots, where every fifth time slot is used to send control messages. This means that a DMA transmissions can only be initiated after the fifth time slot, when the control messages are sent to set up the DMA session (Nichols: Column 3, lines 9-29). The time slots are a schedule.

It would have been obvious to have the circuitry to initiate direct memory access transfer initiates direct memory access transfer in response to a schedule of times to initiate the transfer.

The suggestion/motivation for doing so would have been that allowing DMA transfers only at specific intervals prevents DMA transfers from conflicting with other

system functions. By delaying the transfer of the statistics according to a schedule of time slots, the transfer of the statistics is less likely to cause conflicts with other components, as time slots can be utilized to properly schedule each component.

With regard to claims 2, 18, and 28, Boucher further teaches that at least one statistic comprises at least one of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface (Boucher: Column 56, lines 51-63).

With respect to claim 3, Boucher further teaches circuitry to include a timestamp with the direct memory access transfer of the at least one statistic (Boucher: Column 67, lines 13-26).

With respect to claim 4, Boucher teaches circuitry to include a sequence count with the direct memory access transfer of the at least one statistic, the sequence count distinguishing different sets of the at least one statistic (Boucher: Column 57, lines 6-12. As each DMA transfer is an event, the count can distinguish between different sets of the same statistic).

With respect to claim 5, Boucher teaches that the at least one statistic comprises at least one statistic derived from multiple packets (Boucher: Column 56, lines 41-50. Successful transmits and receives, transmit and receive errors, and transmit collisions are cumulative statistics derived from the transmission of multiple packets.).

With regard to claim 6, Boucher teaches circuitry that is operationally coupled to the direct memory access unit to initiate direct memory access transfer of received network data (Boucher: Column 8, lines 30-37).

With regard to claim 7, Boucher teaches that the network interface comprises a framer (Boucher: Column 56, lines 18-26. To send and receive frames, there must be a framer to create the frames).

With regard to claim 8, Boucher teaches that the network interface comprises a Media Access Controller (MAC) (Boucher: Figure 21, MAC-A to MAC-D).

With regard to claim 9, Boucher teaches that the network interface comprises a PHY (Boucher: Column 77, lines 6-15).

With regard to claims 10 and 35, Boucher teaches circuitry to configure the circuitry to initiate direct memory transfer (Boucher: Column 60, lines 53-59).

With regard to claim 11, Boucher teaches that the circuitry to configure comprises circuitry to respond to at least one of the following: a request to transfer at least one of the at least one statistics (Boucher: Column 63, lines 24-30), an indication of at least one time to initiate a transfer, at least one indication of at least one statistic to transfer, an indication of at least one time to initiate a transfer, at least one indication of at least one statistic to transfer, an indication of the location in memory in which to transfer the at least one statistic, and a schedule of statistic transfers.

With regard to claim 12, Boucher teaches that the circuitry to configure comprises at least one register (Boucher: Column 56, lines 27-33).

With regard to claims 13 and 36, Boucher teaches that the circuitry to configure comprises circuitry to determine configuration information from received packets (Boucher: Column 21, line 64 to column 22, line 10. As the CCB is identified, circuitry is present to determine configuration information from received packets. CCB is defined in column 7, lines 22-30.).

With regard to claim 14, Boucher teaches that the circuitry to determine configuration information from received packets comprises circuitry to intercept packets traveling along a transmit path (Boucher: Column 36, lines 14-20).

With regard to claims 15, 25, and 33, Boucher teaches that the direct memory access unit comprises circuitry to notify a processor of completion of a transfer (Boucher: Column 90, line 64 to column 91, line 12).

With regard to claims 17 and 27, Boucher teaches transferring packets from the network interface to the memory by direct memory access (Boucher: Column 63, lines 18-20. The term frame is interpreted as being synonymous with packet.).

With regard to claims 19, 29, and 38, Boucher teaches transferring at least one of a timestamp and a sequence number with the at least one of the statistics (Boucher: Column 67, lines 13-26).

With regard to claim 20, Boucher teaches that the network interface groups digital bits into frames (Boucher: Column 56, lines 18-26. To send and receive frames, there must be a way to group digital bits into frames).

With regard to claims 21 and 30, Boucher teaches configuring the transfer of at least one of the statistics (Boucher: Column 60, lines 53-59).

With regard to claims 22 and 31, Boucher teaches configuring at least one of the following: at least one subset of the statistics to transfer, at least one time to initiate a transfer, and at least one memory location to receive transferred data (Boucher: Column 84, lines 52-61).

With regard to claim 23, Boucher teaches receiving a packet at the network interface (Boucher: Column 1, lines 40-42) and configuring based on data included in the packet (Boucher: Column 21, line 64 to column 22, line 10. As the CCB is identified, circuitry is present to determine configuration information from data within received packets. CCB is defined in column 7, lines 22-30.).

With regard to claim 24, Boucher teaches that transferring into the memory comprises transferring into a cache memory of at least one of the at least one processor (Boucher: Column 61, lines 14-30).

With regard to claim 32, Boucher teaches instructions for configuring the transfer based on contents of a received packet (Boucher: Column 21, line 64 to column 22, line 10. As the CCB is identified, circuitry is present to determine configuration information from the contents of received packets. CCB is defined in column 7, lines 22-30.).

With regard to claim 37, Boucher teaches circuitry, operationally coupled to the direct memory access unit, to initiate transfer of packets received via the network connection (Boucher: Column 63, lines 18-20. The term frame is interpreted as being synonymous with packet.).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Christensen whose telephone number is (571) 270-1144. The examiner can normally be reached on Monday through Thursday 6:30AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vaughn William can be reached on (571) 272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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